INFORMATION DISCLOSURE CITATION PTO-1449	Customer Number 26615	ATTORNEY'S DKT NO. H1478	APPLICATION NO. Unassigned
		APPLICANT(S) Shibly S. Ahmed et al.	
		FILING DATE DECEMBER 4, 2003	GROUP Unassigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
DN	6,225,173 B1	05-01-01	Yu	438	301	11-06-98
DN	6,413,802 B1	07-02-02	Hu et al.	438	151	10-23-00
DN	6,583,469 B1	06-24-03	Fried et al.	257	329	01-28-02

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DN	Co-pending U.S. Patent Application No. 10/405,342, filed April 3, 2003 entitled: "Method for Forming a Gate in a FinFet Device and Thinning a Fin in a Channel Region of the FinFet Device," 17 page specification; 14 sheets of drawings.
	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 2001 IEEE, IEDM, pages 421-424.
	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
DN	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.

EXAMINER	DATE CONSIDERED
	2/23/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).